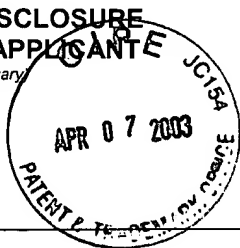


Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**  
(Use as many sheets as necessary)



Complete if Known

Application Number	09/944981
Filing Date	August 30, 2001
First Named Inventor	Ahn, Kie
Group Art Unit	2812
Examiner Name	Lindsay, Walter

Sheet 1 of 3

Attorney Docket No: 1303.021US1

**US PATENT DOCUMENTS**

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
WLL	US2002/0155688	10/24/2002	Ahn, K. Y., et al.	438	592	04/20/2001
WLL	US2002/0155689	10/24/2002	Ahn, K. Y., et al.	29	76	02/11/2002
WLL	US2002/0192974	12/19/2002	Ahn, Kie, et al.	438	722	06/13/2001
WLL	US2003/0017717	01/23/2003	Ahn, Kie, et al.	438	768	07/18/2001
WLL	US-4,399,424	04/16/1983	Rigby, L. J.	338	34	10/05/1981
WLL	US-5,828,080	10/27/1998	Yano, Y., et al.	257	43	04/17/1995
WLL	US-6,495,436	12/17/2002	Ahn, Kie, et al.	438	591	02/09/2001

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T <sup>2</sup>
WLL	JP-2001-332546	11/30/2001		H01L	21/316	

**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		International Technology for Semiconductor Roadmap, (1999),	
WLL		BRIGHT, A A., et al., "Low-rate plasma oxidation of Si in a dilute oxygen/helium plasma for low-temperature gate quality Si/SiO <sub>2</sub> interfaces", <u>Applied Physics Letters</u> , (February 1991), pp. 619-621	
WLL		CHENG, BAOHONG, et al., "The Impact of High-k Gate Dielectrics and Metal Gate Electrodes on Sub-100nm MOSFET's", <u>IEEE Transactions on Electron Devices</u> , (1999), 1537-1544	
WLL		FUYUKI, TAKASHI, et al., "Initial stage of ultra-thin SiO <sub>2</sub> formation at low temperatures using activated oxygen", <u>Applied Surface Science</u> , (1997), pp. 123-126	
WLL		HIRAYAMA, MASAKI, et al., "Low-Temperature Growth of High-Integrity Silicon Oxide Films by Oxygen Radical Generated in High Density Krypton Plasma", <u>IEDM Technical Digest</u> , (1999), 249-252	
WLL		HUBBARD, K. J., et al., "Thermodynamic stability of binary oxides in contact with silicon", <u>J. Mater. Res.</u> , (11/1996), 2757-2776	
WLL		JEONG, CHANG-WOOK, et al., "Plasma-Assisted Atomic Layer Growth of High-Quality Aluminum Oxide Thin Films", <u>Japanese Journal of Applied Physics</u> , (January 2001), pp. 285-289	

EXAMINER

*Walter Lindsay*

DATE CONSIDERED

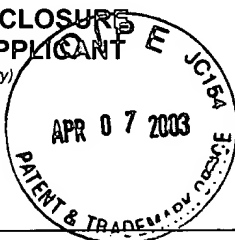
5/1/03

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)



Complete if Known

Application Number	09/944981
Filing Date	August 30, 2001
First Named Inventor	Ahn, Kie
Group Art Unit	2812
Examiner Name	Lindsay, Walter

Sheet 2 of 3

Attorney Docket No: 1303.021US1

WLL	KAWAI, Y, et al., "Ultra-low temperature growth of high-integrity gate oxide films by low-energy ion-assisted oxidation", <u>Applied Physics Letters</u> , (April 1994),pp. 2223-2225	
WLL	KIM, C T., et al., "Application of Al <sub>2</sub> O <sub>3</sub> Grown by Atomic Layer Deposition to DRAM and FeRAM", <u>International Symposium in Integrated Ferroelectrics</u> , (March 2000),pp. 316	
WLL	KIM, Y, et al., "Substrate dependence on the optical properties of Al <sub>2</sub> O <sub>3</sub> films grown by atomic layer deposition", <u>Applied Physics Letters</u> , (December 1997),pp. 3604-3606	
WLL	LESKELA, M, et al., "ALD precursor chemistry: Evolution and future challenges", <u>Journal de Physique</u> , (1999),pp. 837-852	
WLL	LIU, C. T., "Circuit Requirement and Integration Challenges of Thin Gate Dielectrics for Ultra Small MOSFET's", <u>IEDM</u> , (1998),747-750	
WLL	LIU, Y C., et al., "Growth of ultrathin SiO <sub>2</sub> by surface irradiation with an O <sub>2</sub> +Ar election cyclotron resonance microwave plasma at low temperatures", <u>Journal of Applied Physics</u> , (February 1999),pp. 1911-1915	
WLL	MARTIN, P J., et al., "Ion-beam-assisted deposition of thin films", <u>Applied Optics</u> , (January 1983),pp. 178-184	
WLL	MULLER, D. A., "The electronic structure at the atomic scale of ultrathin gate oxides", <u>Nature</u> , vol.399, no.6738, 24 June 1999, (1999),758-61	
WLL	NIEMINEN, MINNA, et al., "Formation and stability of lanthanum oxide thin films deposited from B-diketonate precursor", <u>Applied Surface Science</u> , (2001),pp. 155-165	
WLL	OSTEN, H. J., et al., "High-k Gate Dielectrics with Ultra-low Leakage Current Based on Praseodymium Oxide", <u>IEEE</u> , (2000),653-656	
WLL	PAN, TUNG M., et al., "High Quality Ultrathin CoTiO <sub>3</sub> High-k Gate Dielectrics", <u>Electrochemical and Solid-State Letters</u> , (2000),pp. 433-434	
WLL	PAN, TUNG M., et al., "High-k cobalt-titanium oxide dielectrics formed by oxidation of sputtered Co/Ti or Ti/Co films", <u>Applied Physics Letters</u> , (March 2001),pp. 1439-1441	
WLL	QI, WEN-JIE, et al., "MOSCAP and MOSFET characteristics using ZrO <sub>2</sub> gate dielectric deposited directly on Si", <u>IEDM Technical Digest</u> , (1999),145-148	
WLL	SAITO, YUJI, et al., "Advantage of Radical Oxidation for Improving Reliability of Ultra-Thin Gate Oxide", <u>2000 Symposium on VLSI Technology Digest of Technical Papers</u> , (2000),176-177	
WLL	SAITO, YUJI, et al., "High-Integrity Silicon Oxide Grown at Low-Temperature by Atomic Oxygen Generated in High-Density Krypton Plasma", <u>Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials</u> , (1999),152-153	
WLL	SHIN, CHANG H., et al., "Fabrication and Characterization of MFISFET using Al <sub>2</sub> O <sub>3</sub> Insulating Layer for Non-Volatile Memory", <u>12th International Symposium in Integrated Ferroelectrics</u> , (March 2000),1-9	
WLL	SZE, S M., <u>Physics of Semiconductor Devices</u> , (1981),p. 431	
WLL	SZE, S M., <u>Physics of Semiconductor Devices</u> , (1981),p. 473	

EXAMINER

DATE CONSIDERED

8/11/03

Substitute Disclosure Statement Form (PTO-1449)

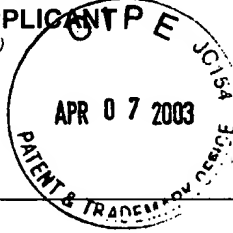
\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)




Complete if Known

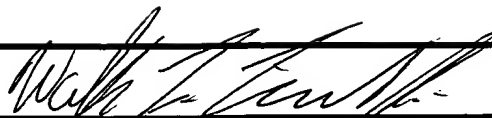
Application Number	09/944981
Filing Date	August 30, 2001
First Named Inventor	Ahn, Kie
Group Art Unit	2812
Examiner Name	Lindsay, Walter

Sheet 3 of 3

Attorney Docket No: 1303.021US1

	WOLF, STANLEY, et al., "Silicon Processing for the VLSI Era - Volume I: Process Technology", Second Edition, Lattice Press, Sunset Beach, California, (2000), page 443
---	--

EXAMINER



DATE CONSIDERED

5/11/03

Substitute Disclosure Statement Form (PTO-1449)

\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached